AMENDMENT TO THE CLAIMS

Please **CANCEL** claims 18-30.

A copy of all pending claims and a status of the claims is provided below.

1. (original) A method for manufacturing a device including an n-type device and a p-type device, comprising:

forming a shallow-trench-isolation oxide (STI) isolating the n-type device from the p-type device;

adjusting the shallow-trench-isolation oxide corresponding to at least one of the n-type device and the p-type device such that a thickness of the shallow-trench-isolation oxide adjacent to the n-type device is different from a thickness of the shallow-trench-isolation oxide adjacent to the p-type device; and

forming a strain layer over the semiconductor substrate.

2. (original) The method of claim 1, wherein the strain layer comprises an etch stop nitride film.

3. (original) The method of claim 1, wherein the strain layer is one of a compressive strain layer or a tensile strain layer.

4. (original) The method of claim 1, wherein the step of adjusting comprises forming a pad nitride with a first thickness for the n-type device and forming a pad

nitride with a second thickness for the p-type device such that the first thickness is different from the second thickness.

5. (original) The method of claim 4, wherein the first thickness is smaller than the second thickness.

6. (original) The method of claim 4, wherein the first thickness is greater than the second thickness.

7. (original) The method of claim 1, wherein the step of adjusting comprises covering the n-type transistor while exposing the semiconductor substrate to at least one oxide etching chemical, such that a thickness of the shallow-trench-isolation oxide adjacent to the n-type device is greater than the thickness of the shallow-trench-isolation oxide adjacent to the p-type device.

8. (original) The method of claim 7, wherein the oxide etching chemical includes HF (hydrofluoric acid).

9. (original) The method of claim 1, wherein the step of adjusting comprises covering the p-type transistor while exposing the n-type transistor and the semiconductor substrate to at least one oxide etching chemical, such that a thickness of the shallow-trench-isolation oxide adjacent to the p-type device is greater than the thickness of the shallow-trench-isolation oxide adjacent to the n-type device.

10. (original) The method of claim 9, wherein the oxide etching chemical includes HF.

11. (original) The method of claim 1, wherein the step of forming a strain layer comprises forming at least one of a SiGe, Si_3N_4, SiO_2 and Sio_xN_y layer on the semiconductor substrate.

12. (original) The method of claim 1, wherein the step of forming a shallow-trench-isolation oxide (STI) isolating the n-type device from the p-type device comprises forming the shallow-trench-isolation oxide at a distance of about 1500 Angstroms or less from the adjacent n-type device or p-type device.

13. (original) The method of claim 1, wherein the thickness of the shallow-trench-isolation oxide of one of the n-type device or the p-type device is about 300 Angstroms to about 1000 Angstroms less than the shallow-trench-isolation oxide of the other of the n-type device or the p-type device.

14. (original) A method for manufacturing a device including an n-type device and a p-type device, comprising:

forming a boundary for the n-type device and the p-type device;

adjusting a height of the boundary such that a boundary adjacent to the n-type device is at a level which is different from a level of a height of a boundary adjacent to the p-type device; and

forming a strain layer over the semiconductor substrate.

15. (original) The method of claim 14, wherein the strain layer comprises a compressive strain layer or a tensile strain layer.

16. (original) The method of claim 15, wherein:

the strain layer is a tensile strain layer, and

the height of the boundary adjacent to the n-type device is lower than the height of the boundary adjacent to the p-type device.

17. (original) The method of claim 16, wherein:

the strain layer is a compressive strain layer, and

the height of the boundary adjacent to the p-type device is lower than the height of the boundary adjacent to the n-type device.

Claims 18-30. (cancel)